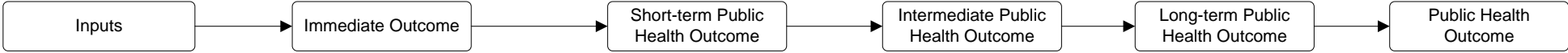


Overview Logic Model



DRAFT

