**UNITED STATES DEPARTMENT OF COMMERCE**
**National Institute of Standards and Technology**
Gaithersburg, Maryland 20899-
OFFICE OF THE DIRECTOR

Dr. Dominic J. Mancini, Ph.D.
Deputy Administrator
Office of Information and Regulatory Affairs
Office of Management and Budget
Washington, DC 20503

Dear Dr. Mancini,

I am requesting emergency approval of a new information collection that is essential to the mission of the Department of Commerce—namely, the swift and robust implementation of the CHIPS Act of 2022 (Division A of P.L. 117-167) (the Act). I have determined that collecting this information promptly, prior to expiration of the ordinary time periods established in the Paperwork Reduction Act, is necessary to prevent public harm that would be reasonably likely to result if those time periods were followed. *See* 44 U.S.C. 3507(j); 5 C.F.R. 1320.13(a).

The Act tasks the Secretary of Commerce with carrying out section 9906 of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (15 U.S.C. 4656). This statute aims to catalyze long-term growth in the domestic semiconductor industry in support of U.S. economic resilience and national security. An expeditious collection of this information is needed in conjunction with a site selection process that will be used to identify a flagship research and development prototyping and packaging facility that is anticipated to become the linchpin of both the National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP), the two largest CHIPS research and development programs established by Congress. The information is important for the Department of Commerce and Natcast—the purpose-built nonprofit entity which serves as the operator of the NSTC, and which is anticipated to serve as the operator of this flagship facility—in order to establish at the outset of the site selection process which states and/or territories have existing semiconductor ecosystems that could support this facility.

Both the NSTC and NAPMP have an urgent need to identify facilities in order to accomplish their statutory missions, which are fundamentally economic and national security missions. The NSTC is required "to conduct advanced semiconductor manufacturing, design and packaging research, and prototyping that strengthens the entire domestic ecosystem." 15 U.S.C. 4656(c)(2)(A). The NSTC is expected to "significantly reduce the time and cost of moving from design idea to commercialization through access to shared facilities, digital assets and technical expertise for advancing design, prototyping, manufacturing, packaging, and scaling of semiconductors and semiconductor-related products."[1] The NAPMP is expected to "include an Advanced Packaging Piloting Facility (APPF) where successful development efforts will be transitioned and validated for scaled transition to U.S.

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[1] CHIPS Research and Development Office, National Institute of Standards and Technology, U.S. Department of Commerce, *A Vision and Strategy for the National Semiconductor Technology Center*, available at https://www.nist.gov/system/files/documents/2023/04/26/NSTC-Vision-Strategy-Fact-Sheet.pdf-Vision-Strategy-Fact-Sheet.pdf (published Apr. 25, 2023).

manufacturing. This is a key facility for technology transfer to high-volume manufacturing."[2] The Department of Commerce and Natcast have determined that co-locating many NSTC- and NAPMP-related capabilities in a single facility would be a significant added value to both programs. Having state-of-the-art semiconductor research and development capabilities in the same location as advanced packaging capabilities would be transformative for the semiconductor ecosystem in the United States, because the boundaries between semiconductor wafer/chip processing and next generation advanced packaging are blurring. Today, technology and researchers in these different domains are separated, and no independent research facilities for such innovations in packaging exist in the United States. A flagship facility with co-located chip/package solutions would accelerate co-optimized solutions at a pace that is not currently possible and set the United States on a path for continued leadership—at a time when public and private investment in semiconductor research and development by foreign adversaries is substantially increasing.

Today, many elements of the semiconductor ecosystem are geographically concentrated and produced outside of the United States, which is especially true of many advanced packaging capabilities. This endangers the global economy and U.S. national security. For example, many U.S. defense capabilities—including hypersonic weapons, drones, and satellites—are unduly vulnerable to supply chain disruptions and competing advances in research and development. To strengthen U.S. economic and national security, the CHIPS research and development programs must have these facilities online in an expeditious manner.

Congress appropriated $11 billion to fund CHIPS research and development programs. It is anticipated that the single biggest investment of that $11 billion will be allocated to NSTC and NAPMP facilities, which are critically important to the success of both of programs. Given the scale of the investment, the funding needed to acquire and operate this research and development prototyping and packaging facility will have implications on the entirety of the CHIPS research and development budget, further underscoring the importance of the collection to inform this process launching in the very near future.

The information collection will take the form of a voluntary Ecosystem Questionnaire for States and Territories to Inform CHIPS R&D Facility Site Selection Process. The Questionnaire will pose identical questions to Economic Development Organizations (EDOs) in all 56 states, territories, and the District of Columbia.[3] The Ecosystem Questionnaire will request information regarding the extent to which a state or territory can demonstrate: the presence of entities from the semiconductor value chain; a semiconductor workforce and current workforce development programs; semiconductor-related advanced education and research programs; significant state, local, and private investment in the semiconductor ecosystem; and state incentives for semiconductor research and development. The Ecosystem Questionnaire is also structured to be as minimally burdensome as possible because, among other reasons: responses are predominantly requested in the form of multiple-choice answers, the information the Questionnaire solicits should be easily available to EDOs, EDOs will be given advance notice to expect the Questionnaire, and the Department has published a Federal Register notice providing a period for public comment. This will be a one-time collection of information available to all 56 states, territories,

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[2] CHIPS Research and Development Office, National Institute of Standards and Technology, U.S. Department of Commerce, *The Vision for the CHIPS for America National Advanced Packaging Manufacturing Program*, p. 3, available at https://www.nist.gov/system/files/documents/2023/11/19/NAPMP-Vision-Paper-20231120.pdf (published Nov. 19, 2023).

[3] This collection is subject to the Paperwork Reduction Act as the Ecosystem Questionnaire would pose identical questions to all 56 states, territories, and the District of Columbia. *See* 5 C.F.R. 1320.3(c)(4) and 1320.3(k).

and the District of Columbia. Only states or territories that submit responses to the Ecosystem Questionnaire will be considered for selection of this facility.

The Department is requesting emergency approval of the Ecosystem Questionnaire for States and Territories to Inform CHIPS R&D Facility Site Selection Process by July 15, 2024. Prompt collection of the information sought in the Questionnaire is necessary to avert public harm. In particular, because both Congress and the Administration have identified American leadership in semiconductor research and development as a matter of national security and defense, the Department is implementing the search for this facility on an expedited timeline to meet economic and national security needs that Congress has identified. The Department needs to obtain the requested information from EDOs as expeditiously as possible in order to meet its statutory obligations under the CHIPS Act to provide an appropriate facility for both the NSTC and NAPMP programs, while the appropriated funds continue to be available for this purpose.

Additionally, adherence to the ordinary timelines of the Paperwork Reduction Act could jeopardize NSTC and its economic and national security mission more broadly. Congress required the Departments of Commerce and Defense to establish the NSTC as a public-private consortium with participation from the private sector, the Department of Energy, and the National Science Foundation. *See* 15 U.S.C. 4656(c)(1). Private participation is voluntary, yet critical to ensure NSTC's ability to meet its statutory missions, including strengthening the domestic semiconductor ecosystem. *See* 15 U.S.C. 4656(c)(2)(A). And, as noted, a state-of-the-art prototyping and packaging facility is expected to be vital to NSTC's success and a marquee benefit for private participants. Natcast is required to ensure that potential members of the NSTC are eligible to join the public-private sector consortium in fall 2024; thus, it is especially important to the Department and Natcast to be able to make significant progress on the site selection for this facility in order to demonstrate the expected value of the NSTC to potential members. The three- or four-month delay that would result if an emergency clearance was not granted would undermine NSTC's national and economic security missions and would cause broader harm to the Department's ability to meet Congress's expectations under the CHIPS Act.

Please contact Liz Reinhart (elizabeth.reinhart@nist.gov) if you or your staff have any questions regarding this request.

Sincerely,

LAURIE LOCASCIO

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Laurie E. Locascio, Ph.D., NAE
Under Secretary of Commerce for Standards and Technology &
Director, National Institute of Standards and Technology